PATENT

DOCKET NO. 5231.16

#18/1
LDT
2-21-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED entered
FEB - 4 2002
Technology Center 2100

Applicant(s): John S. Yates Jr., et al.
Serial No.: 09/429,094
Filed: October 28, 1999
Title: SIDE TABLES ANNOTATING AN INSTRUCTION STREAM
Art Unit: 2155
Examiner: D. Eng

COMMISSIONER FOR PATENTS
Box AF
Washington D.C. 20231

RESPONSE TO OFFICE ACTION OF DECEMBER 4, 2001

Kindly amend the application as follows.

In the claims:

Kindly amend the claims as follows.

19. (twice amended) A microprocessor chip, comprising:

instruction pipeline circuitry; and

interrupt circuitry cooperatively designed with the instruction pipeline circuitry to trigger an interrupt on execution of an instruction of a process in accordance with synchronous interrupt criteria, the interrupt criteria being based at least in part on a memory state of the computer and the address of the instruction, wherein the architectural definition of the instruction in an emulated architecture does not call for an interrupt.

Kindly add the following new claim:

58. (new) The microprocessor chip of claim 19, wherein the interrupt criteria are further based on the value of the instruction.

I certify that this correspondence, along with any documents referred to therein, is being transmitted by facsimile on February 4, 2002 to The Commissioner for Patents, Box AF, Washington D.C. 20231.

David E. Boaz